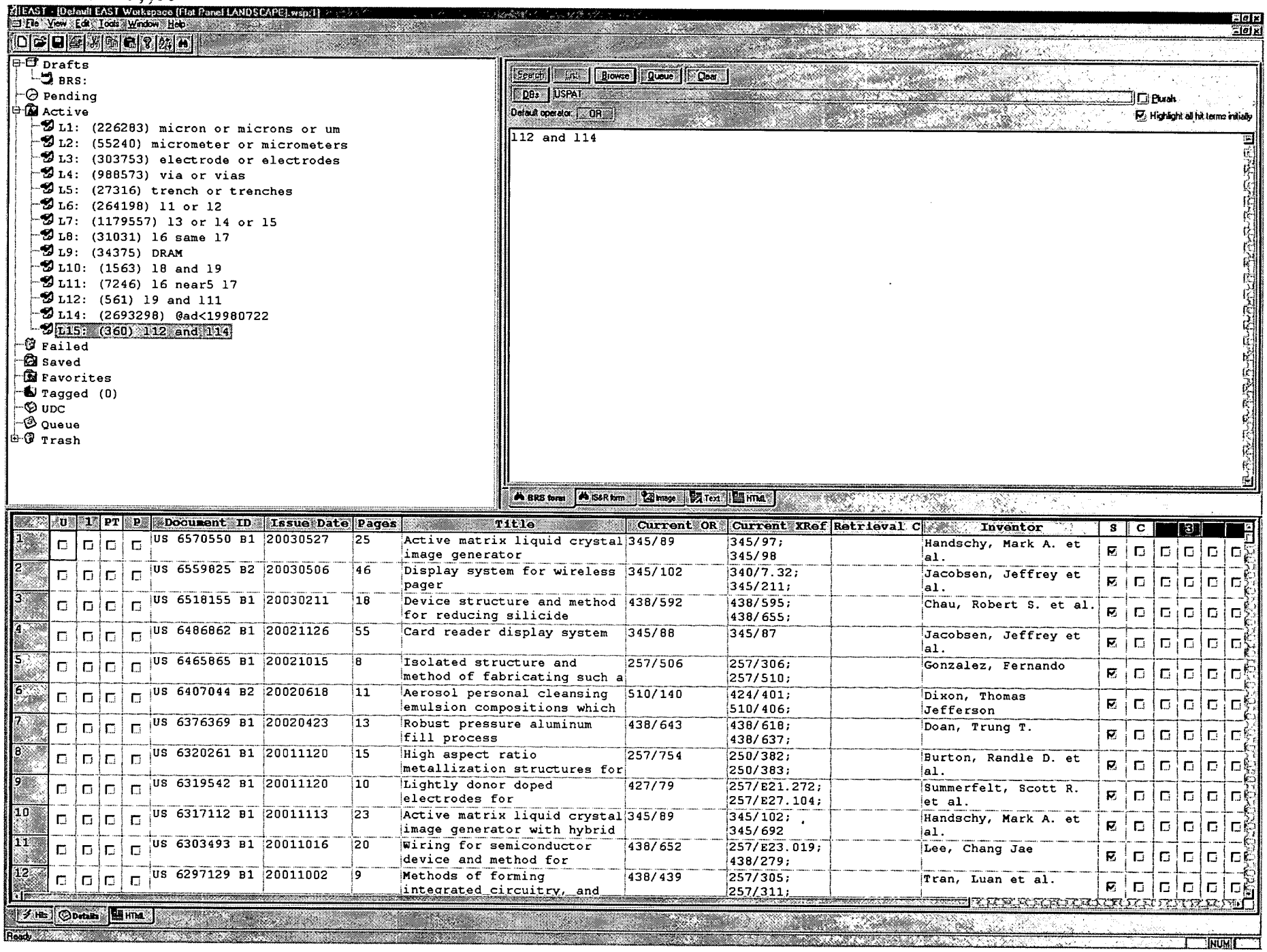

	U	1	PT	P	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	3
1	☐	☐	☐	☐	US 6570550 B1	20030527	25	Active matrix liquid crystal image generator	345/89	345/97; 345/98		Handschy, Mark A. et al.	☑	☐	☐
2	☐	☐	☐	☐	US 6559825 B2	20030506	46	Display system for wireless pager	345/102	340/7.32; 345/211;		Jacobsen, Jeffrey et al.	☑	☐	☐
3	☐	☐	☐	☐	US 6518155 B1	20030211	18	Device structure and method for reducing silicide	438/592	438/595; 438/655;		Chau, Robert S. et al.	☑	☐	☐
4	☐	☐	☐	☐	US 6486862 B1	20021126	55	Card reader display system	345/88	345/87		Jacobsen, Jeffrey et al.	☑	☐	☐
5	☐	☐	☐	☐	US 6465865 B1	20021015	8	Isolated structure and method of fabricating such a	257/506	257/306; 257/510;		Gonzalez, Fernando	☑	☐	☐
6	☐	☐	☐	☐	US 6407044 B2	20020618	11	Aerosol personal cleansing emulsion compositions which	510/140	424/401; 510/406;		Dixon, Thomas Jefferson	☑	☐	☐
7	☐	☐	☐	☐	US 6376369 B1	20020423	13	Robust pressure aluminum fill process	438/643	438/618; 438/637;		Doan, Trung T.	☑	☐	☐
8	☐	☐	☐	☐	US 6320261 B1	20011120	15	High aspect ratio metallization structures for	257/754	250/382; 250/383;		Burton, Randle D. et al.	☑	☐	☐
9	☐	☐	☐	☐	US 6319542 B1	20011120	10	Lightly donor doped electrodes for	427/79	257/E21.272; 257/E27.104;		Summerfelt, Scott R. et al.	☑	☐	☐
10	☐	☐	☐	☐	US 6317112 B1	20011113	23	Active matrix liquid crystal image generator with hybrid	345/89	345/102; 345/692		Handschy, Mark A. et al.	☑	☐	☐
11	☐	☐	☐	☐	US 6303493 B1	20011016	20	Wiring for semiconductor device and method for	438/652	257/E23.019; 438/279;		Lee, Chang Jae	☑	☐	☐
12	☐	☐	☐	☐	US 6297129 B1	20011002	9	Methods of forming integrated circuitry, and	438/439	257/305; 257/311;		Tran, Luan et al.	☑	☐	☐

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12	US 6303493 B1	20							☑				USPAT
13	US 6297129 B1	9							☑				USPAT
14	US 6262449 B1	10							☑				USPAT
15	US 6261883 B1	43							☑				USPAT
16	US 6259127 B1	11							☑				USPAT
17	US 6236079 B1	28							☑				USPAT

Detailed Description Text - DETX (9):

With reference to FIG. 5D, a pad oxide layer 210 of silicon dioxide (SiO.sub.2) and a pad nitride layer 212 of silicon nitride (Si.sub.3 N.sub.4) are successively formed on the surface of epitaxial silicon layer 208. Pad oxide layer 210 may be formed by thermal oxidization (e.g., 900.degree. C. in an atmosphere of dry O.sub.2) and may have a thickness of about 10 nanometers. Pad nitride layer 212 may be formed by chemical vapor deposition and may have a thickness of about 100 nanometers. Shallow trenches 214 are then formed in epitaxial layer 208 using a patterned resist (not shown) and an etching process such as reactive ion etching (RIE). The dimensions of the shallow trenches are dependent upon feature size. For example, for a 1 Gbit DRAM, shallow trenches 214 may have a width of 0.15 micrometers (.mu.m) and a depth of 0.15 micrometers (.mu.m). An insulating layer of, for example, TEOS, is then blanket deposited over the surface of pad nitride layer 212 and in shallow trenches 214. The insulating layer is then etched back using, for example, CMP and RIE, with pad nitride layer 212 serving as a stopper layer, whereby shallow trench isolation structures 108 which define the active areas AA are formed.

Detailed Description Text - DETX (17):

In the second embodiment, deep trenches 110' are oriented in a direction which is orthogonal to the direction in which the deep trenches 110 are oriented in the first embodiment. Because of this, forming the semiconductor memory device of FIGS. 6 and 7 using the method described with respect to FIGS. 5A-5J will cause the transfer transistors to be formed in the portion of the epitaxial layer over the deep trench. As noted above, this portion of the epitaxial layer may have defects which could adversely affect the operation of the transfer transistors. In order to provide a high quality epitaxial layer in which to form the transfer transistors, the epitaxial layer may be subjected to a high temperature annealing process (e.g., at a temperature of about 1100.degree. C. in an atmosphere of N.sub.2). Alternatively, a laser or an electron beam anneal may be used. In still another alternative embodiment, a wafer bonding technique such as that shown in FIG. 8 may be utilized. Specifically, a first silicon wafer 302 having the trench capacitors formed therein is bonded to a second silicon wafer 306 having shallow trench isolation regions 108 formed therein. Second silicon wafer 306 is then polished by, for example, chemical mechanical polishing (CMP) to provide a silicon layer 308 having a thickness of, for example, about 0.15 micrometers (.mu.m) for a 1 Gbit DRAM. The process steps of FIGS. 5E-5J may then be carried out to form the semiconductor memory device of FIGS. 6 and 7. In this way, the problems associated with low quality epitaxial films grown over the deep trenches can be avoided.

Detailed Description Text - DETX (19):

Table 1 provides a cell comparison for the first generation of 1 Gbit DRAM devices having a 0.18 micron design rule. As can be seen from the data set forth in Table 1, DRAM devices manufactured in accordance with the embodiments of the present invention provide the same capacitance as scaled down cells manufactured in accordance with the MINT architecture shown in FIGS. 1A and 1B of this patent application, while at the same time providing trenches with smaller aspect ratios within which the capacitors are formed. Specifically, 1 Gbit memory cells in accordance with the first and second embodiments of the present invention have trench capacitors formed in trenches with aspect ratios which are 28% less than the aspect ratio of the trenches for 1 Gbit memory cells based on scaling down the current MINT architecture. Memory cells in accordance with the third embodiment of the present invention have trench

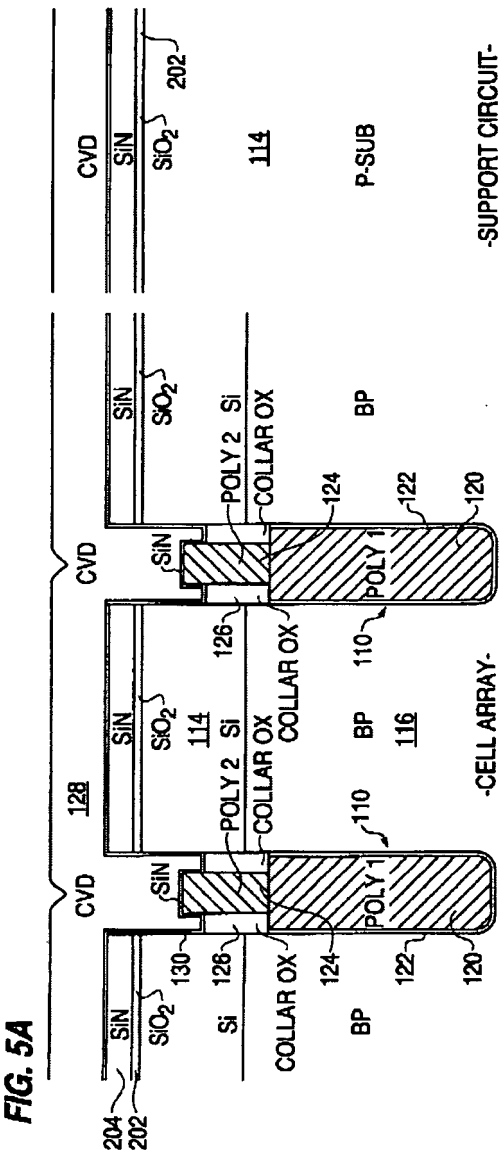

FIG. 5A

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		Document ID	Pages	1		3			U	S	C	P	Kind Codes	Sou
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21	US	6211034	B1	9										USPAT
22	US	6204069	B1	9										USPAT
23	US	6191470	B1	20										USPAT
24	US	6188120	B1	9										USPAT
25	US	6187622	B1	23										USPAT

Detailed Description Text - DETX (3):
A first embodiment of the present invention will be described below with reference to FIG. 1 through FIG. 7. FIG. 1 through FIG. 7 are partial sectional views sequentially showing the method for production of DRAM in the first embodiment of the present invention.

Detailed Description Text - DETX (61):
In the sixth step shown in FIG. 7, a second inter-layer insulation film 117, a first aluminum wiring layer 118, a protective film 119, a second aluminum wiring layer 120, etc. in the upper portion of the capacitor are formed in methods similar to those of the prior art, thereby the DRAM of one embodiment of the present invention can be obtained.

Detailed Description Text - DETX (62):
In the device made as shown in FIG. 7, separation width between adjacent lower electrodes 114 is decreased to within 0.2 .mu.m because of the large scale of integration and even when the area of the lower electrode 114 projected onto principal plane is made as small as 0.15 square micrometers or smaller, for example, opposing area of the electrodes can be secured by setting the height of the lower electrodes 114 equal to the separation width or greater, and therefore required amount of electric charge can be stored in the capacitor.

Detailed Description Text - DETX (69):
It needs not to say that the present invention is effective for devices other than DRAM having thin film capacitors which employ high dielectric constant film.

Detailed Description Text - DETX (71):
A second embodiment of the present invention will now be described below with reference to FIG. 14 through FIG. 20. FIG. 14 through FIG. 20 are partial sectional views sequentially showing the method for production of DRAM in the second embodiment of the present invention.

Detailed Description Text - DETX (100):
In the sixth step shown in FIG. 20, a second inter-layer insulation film 217, a first aluminum wiring layer 218, a protective film 219, an aluminum wiring layer 220, etc. in the upper portion of the capacitor are formed in methods similar to those of the prior art, thereby to form the DRAM of one embodiment of the present invention.

Detailed Description Text - DETX (101):
In the device made as shown in FIG. 20, separation width between adjacent lower electrodes 214 is decreased to within 0.2 .mu.m because of the large scale of integration and even when the area of the lower electrode 214 projected onto the principle plane is made as small as 0.15 square micrometers or smaller, for example, opposing area of the electrodes can be secured by increasing the height of the lower electrodes 214 to the separation width or greater, and therefore required amount of electric charge can be stored in the capacitor.

ruthenium, iridium, platinum, palladium, rhodium or rhenium, or a compound thereof as the material.

According to this embodiment, a metal ruthenium film having a thickness of 400 nm was formed as the lower electrode 114 by heating the semiconductor substrate 101 to 400° C. in the sputtering process.

While the semiconductor substrate may not necessarily be heated, in case it is heated, the temperature is preferably within 850° C.

Thickness of the lower electrode 114 is preferably such as the effect of making a practical increase in the capacitance is recognized, and within a range from 200 nm to 800 nm in consideration of the machining accuracy.

In the third step shown in FIG. 3, a slot is made by reactive ion etching to separate adjacent capacitor lower electrodes 114 by a space of 0.2 μm. As the height of the lower electrode 114 is 400 nm, the ratio of height to separation width is 2. Size of the capacitor lower electrode 114 is determined so that the projected area onto horizontal plane is from 0.25 μm×0.60 μm (maximum area 0.15 μm²) to 0.07 μm×0.14 μm (minimum area 0.0098 μm²). While separation width is set to 0.2 μm in this embodiment, it can be selected from a range of 0.2 μm to 0.05 μm.

In the fourth step shown in FIG. 4, $SrTiO_3$ film is deposited to form the capacitor insulation film 115 which has perovskite type crystal structure. In this embodiment, the CVD process is employed in forming the capacitor insulation film 115 in consideration of coverage of the side face of the lower electrode. Thickness of the film is 50 nm in this embodiment. Although the capacitor insulation film 115 covers the capacitor lower electrode 114 and is formed also in the slot of the separating portion, part of the slot remains as a step because the separation width is 0.2 μm and thickness of the capacitor insulation film 115 is 50 nm.

The step after forming the capacitor insulation film 115 becomes very narrow and deep, 0.1 μm in width and 0.4 μm in height thus having an aspect ratio of 4.

In the fifth step shown in FIG. 5, the capacitor upper electrode 116 is formed to cover the capacitor insulation film 115 and fill the step.

The capacitor upper electrode 116 is made of such a metal as ruthenium, iridium, platinum, palladium, rhodium or rhenium, or a compound thereof. First a case of forming a metal ruthenium film by the sputtering process as the capacitor upper electrode 116 will be described below. Major sputtering conditions are as follows (these conditions will be called the standard conditions hereafter).

Substrate temperature: 400° C.
Introduced gas: Argon, oxygen
Proportion of gases: Argon: Oxygen=9:1
RF power: 1.25 W/cm²
Vacuum before film formation: Within 1×10^{-5} Torr
Gas pressure: 3 mTorr
Target: Metal ruthenium
Film forming speed: 15 nm/minute

Because the film is formed in an atmosphere of a pressure from 0.5 to 5 mTorr by using a gas comprising argon gas, which is typically used in the sputtering of single metals, and oxygen added in the proportion of 0.1 to 20% in flow rate (oxygen content in the film is 1 to 0.01%), chemical etching mechanism of forming a volatile oxide due to the action of oxygen plasma and sputter etching mechanism by argon ions proceed concurrently. By controlling the degree of vacuum before film formation at 1×10^{-5} Torr, unevenness in the oxygen content caused by residual oxygen which leads to poor reproducibility can be prevented. As the volatile oxide

can easily decompose and deposit on the substrate again, a film of good step coverage can be made in a mechanism similar to the CVD process notwithstanding of the sputtering process, thus making it possible to fill a very narrow slot.

The method of forming the upper electrode 116 will be described with reference to FIG. 9A through FIG. 9C. Because of the directivity of sputtered particles in normal sputtering film formation, it is difficult to form a film over a very narrow slot with high coverage as shown in FIG. 9A. However, because argon gas causes the so-called reverse sputtering effect as the mean free path becomes longer in the case of sputtering at a low pressure, film at a corner which is formed near the microscopic slot is sputter-etched in preference, while a part thereof deposits again in the direction of the bottom of the microscopic slot, and the formation of an overhang on the microscopic slot is prevented. Further, configuration shown in FIG. 9B is obtained by adding the effect of film formation by ruthenium tetraoxide vapor generated in the sputtering of ruthenium with the addition of oxygen. When the sputtering is continued in similar environment, final configuration shown in FIG. 9C is obtained.

Proportion of oxygen flow rate is controlled by means of the rate of film formation, while the oxygen flow rate must be decreased when the rate of film formation is slow and the oxygen flow rate must be increased when the rate of film formation is high (0.1% suffices at about 10 nm/minute but about 20% is required at 400 nm/minute). Etching/film formation ratio can be controlled to 1:5 to 1:3 by controlling the proportion of oxygen flow rate as described above.

In case decomposition of volatile oxide takes place only near the aperture, not near the bottom of the microscopic slot, namely when the slot is very narrow and deep (0.4 to 0.8 μm in depth and 0.05 to 0.15 μm in width), filling by the generation of the volatile oxide may not occur effectively. In this case, modifying the etching/film formation ratio to increase the etching rate from 1:5–1:3 described above to 1:3–1:2 (increase the oxygen gas added) or adding 10% or less of halogen gas such as chloride to the gas phase will solve the problem. Added halogen gas assists the formation of a volatile oxide and suppresses the decomposition thereof.

Now a method of forming a ruthenium dioxide film, which is a compound of ruthenium, as the upper electrode 116 by the sputtering process will be described below. Major sputtering conditions are as follows.

Substrate temperature: 200° C.
Introduced gas: Argon, oxygen
Proportion of gases: Argon: Oxygen=5:5
RF power: 2.5 W/cm²
Vacuum before film formation: Within 1×10^{-5} Torr
Gas pressure: 3 mTorr
Target: Metal ruthenium
Film forming speed: 20 nm/minute

In this embodiment, ruthenium dioxide is deposited by the reactive sputtering process wherein metal ruthenium is used as the target and argon and oxygen are used as major components of the sputtering gas. Sputtering conditions for forming the upper electrode 116 in this embodiment are gas pressure of 0.5 mTorr to 5 mTorr and ratio of film forming rate to etching rate in a range from 2:1 to 5:1.

Oxygen has an effect of accelerating the generation of volatile ruthenium tetraoxide in plasma, and turns a part of ruthenium dioxide film which has been formed into ruthenium tetraoxide, thereby performing chemical etching effect. Because ruthenium tetraoxide which has been gen-

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10	US 6319542 B1	10							☑				USPAT
11	US 6317112 B1	23							☑				USPAT
12	US 6303493 B1	20							☑				USPAT
13	US 6297129 B1	9							☑				USPAT
14	US 6262449 B1	10							☑				USPAT

oxide areas 12 are also formed (labeled 16' in FIG. 1) that interconnect the gate electrodes 16 to the appropriate peripheral circuits on the DRAM chip. Typically the polysilicon layer is deposited by low pressure chemical vapor deposition using, for example, a reactant gas such as silane (SiH.sub.4). The silicide layer is typically formed from a refractory metal, such as tungsten (W). The tungsten silicide (SiW.sub.2) can be formed by a variety of methods which include co-evaportion, co-sputtering, but is now typically deposited by chemical vapor deposition using tungsten hexafluoride (WF6) as the reactant gas. The thickness of the polysilicon layer is preferably between about 500 to 2000 Angstroms, and the thickness of the silicide is preferably between about 500 to 2000 Angstroms. Lightly doped self-aligned source/drain areas 20 are formed next adjacent to the gate electrode 16 using the gate electrodes as part of the implant mask, and implanting an N-type dopant species such as arsenic (As.sup.75) or phosphorus (P.sup.31) in the device areas. For example, a typical implant might consist of phosphorus P.sup.31 at a dose of between 1 E 13 to 10 E 13 atoms/cm.sup.2 and an energy of between about 30 to 80 Kev.

Detailed Description Text - DETX (6):

The remainder of this embodiment relates now more specifically to the method of this invention for fabricating the pillar shaped stacked capacitor, which can further increase the DRAM cell density. The method involves forming a pillar shaped bottom electrodes that extend vertical upward over the FET source/drain contact areas (capacitor node contacts) and requiring very little lateral area in the cell area. The bottom electrode is formed from a single masking level which also forms the capacitor node contact.

Detailed Description Text - DETX (11):

The polysilicon layer 30 is now oxidized to the surface of the insulating layer 28, as depicted in FIG. 5, resulting in the formation of unoxidized doped polysilicon pillars 40 remaining in the node contact openings 7. The polysilicon pillars 40 forms the bottom electrodes for the pillar-shaped stacked capacitor and also provides the capacitor node contacts to the source/drain contact areas 24 of the cell FETs. As is also clearly seen in FIG. 5, the oxidation of layer 30 also results in an array of pillar-shaped bottom electrodes that are electrically isolated from each other, only one of which is shown in FIG. 5. Since the bottom electrode 30 extend vertically upward, the electrodes occupy a very small area on the substrate. This pillar like capacitors will become increasing important in future DRAM cells where the width of the FET gate electrode is expected to be less than a quarter micrometer (um) and the cell area is substantially reduced. The oxidation of polysilicon layer 30 is preferably done in a oxidation furnace using steam oxidation (wet oxidation) for a time sufficient to convert all the polysilicon over the insulating layer 28 to a silicon oxide. By way of example only, if the thickness of polysilicon layer 30 is about 1000 Angstroms, and a wet oxidation is used, then the conversion of the doped polysilicon to oxide can be accomplished at a temperature of about 875 to 900.degree. C. for a time of between about 40 to 60 minutes. Alternatively, the oxidation time can be considerably shortened or the oxidation temperature reduced by using high pressure oxidation, thereby increasing wafer throughput and reducing the processing time. The high pressure oxidation is described in "Silicon Processing for the VLSI Era" Vol. 1, by S. Wolf and R. Tauber, Lattice Press, 1987.

Detailed Description Text - DETX (13):

The array of pillar-shaped stacked capacitors for the DRAM cells are now

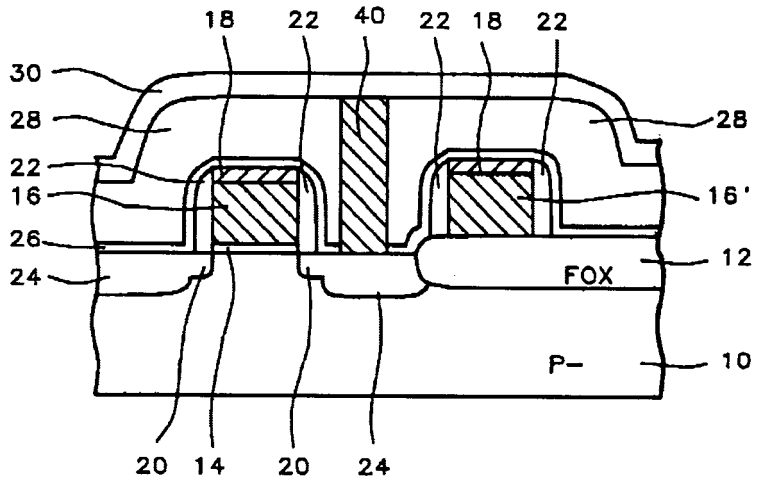

FIG. 5

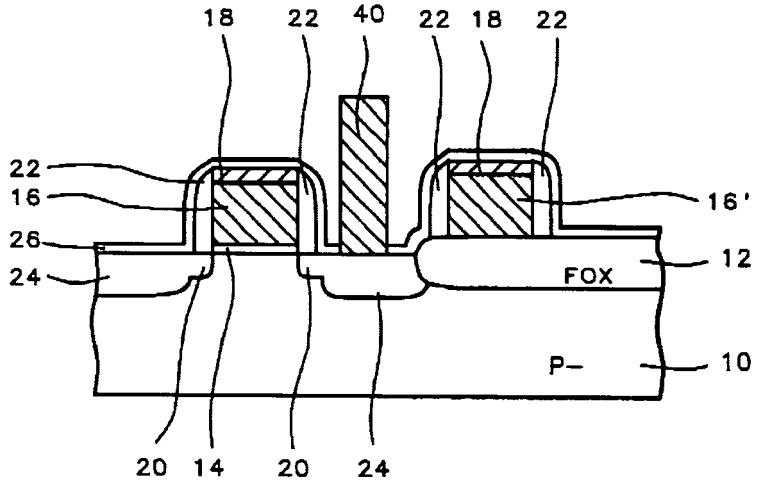

FIG. 6

GAU 5801/1713

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16	US 6259127 B1	11							☑				USPAT

US-PAT-NO: 6259127

DOCUMENT-IDENTIFIER: US 6259127 B1

TITLE: Integrated circuit container having partially rugged surface

ch 1 (12) High Amp DRAMS

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Application Filing Date - AD (1):
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Brief Summary Text - BSTX (5):
FIG. 1, for example, illustrates a container capacitor structure 10 for a DRAM memory cell. An insulating or dielectric layer 12, such as boron phosphosilicate glass (BPSG), is planarized and patterned with a photolithographic mask. The dielectric layer 12 is then etched through the resist mask 24 between a pair of gate electrodes 14 to an underlying silicon substrate, thus forming the container structure 10. The etch may select against nitride insulation of the gate electrodes 14, for example, including nitride sidewall spacers 22. The container 10 is essentially A a cylindrical cavity, but it is illustrated in FIG. 1 in schematic cross-section, for simplicity, without showing the backwall of the cylinder. A conductive layer (not shown in FIG. 1) would then be conformally deposited over the walls of the container 10 to serve as the bottom plate. The interlayer dielectric and top plate would be successively deposited over the bottom plate, forming a capacitor.

Brief Summary Text - BSTX (7):
At the same time, the formation of HSG also increases the thickness of the bottom plate, generally by more than 500 .ANG. and often closer to 600 .ANG.. For the container structure 10 of FIG. 1, this added thickness over the container walls still leaves adequate space within the container 10 for additional layers in an upper portion 19. The added thickness may become critical, however, at a bottom portion 20 of the container 10, which is narrowly confined between the gate electrodes 14. In high-density DRAM chips, the pair of gate electrodes 14 are less than 0.35 microns (3,500 .ANG.) apart. Sidewall spacers 22, which isolate the gate electrodes 14 from the capacitor to be formed, occupy 700 .ANG. on either side of the container 10 cross-section, leaving a diameter of only about 2,100 .ANG. for the remainder of the capacitor structure within the bottom portion of the container 10. These 2,100 .ANG. may easily be filled by the bottom plate to be formed of an amorphous or polysilicon layer (about 500 .ANG. around the container circumference) and the HSG formed over the silicon layer (about 600 .ANG.). These thicknesses represent reductions in the radius of the container and must be doubled in calculating the reduction of the container diameter.

Detailed Description Text - DETX (2):
Although the present description focuses on the context of a DRAM cell, it will be understood that the present invention may have utility in many applications where a conductive layer of rough or high surface area is desired. Such applications include capacitors of all sorts, and especially capacitors

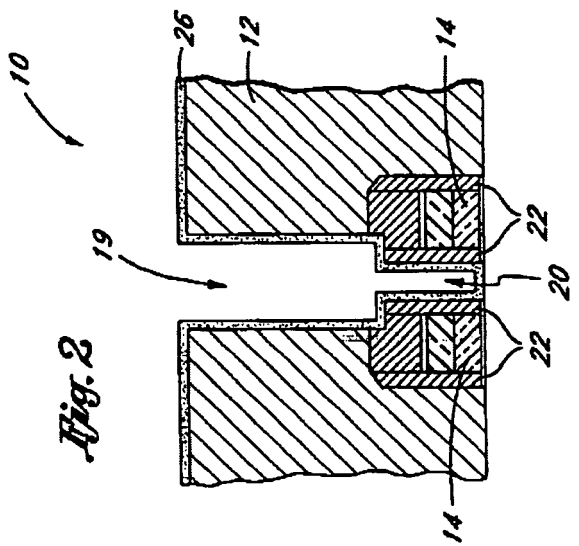

Fig. 2

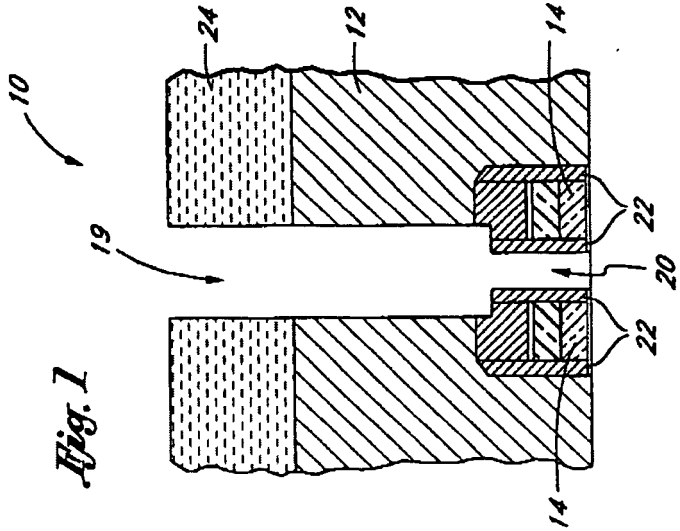

Fig. 1

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1	US 6187152 B1	21								USPAT
2	US 6183611 B1	21								USPAT
3	US 6165956 A	8								USPAT
4	US 6099702 A	5								USPAT
5	US 5965679 A	25								USPAT
6	US 5907791 A	11								USPAT
7	US 5865657 A	22								USPAT

Brief Summary Text - BSTX (7):

One problem with this system is that often substantial time (e.g., minutes) elapses between the electroplating in the plating cell and the rinsing while the system awaits availability of a rinse cell, a transport system, or a human operator. Substantial time may elapse when, for example, there is throughput bottleneck in the rinse stage. During this time, solution molecules may stay attached to the wafer due to the relatively low surface energy of the solution. This allows the solution, in some cases, to chemically react with the elements of the wafer, particularly metallic elements. For example, a water-based salt solution tarnishes a copper work piece if exposed even for a short time. As circuit feature dimensions progress farther into the submicron range, such tarnishing can significantly reduce die yields.

Brief Summary Text - BSTX (12):

The following occurs within this single plating cell. A wafer is first electroplated by lowering the wafer holder to a position in the inner plating bath container that is below a plating solution level. After electroplating, the wafer is raised out of the plating bath and spun so that the spun-off water and plating solution enters the reclaim or waste inlets. When the spun-off water and plating solution enters the waste inlet, a relatively large volume of rinse solution (e.g., 10 milliliters or more) can be applied (e.g., sprayed) onto the wafer to thoroughly rinse the wafer . The wafer can also be subsequently dried by spinning the wafer at a relatively fast spin rate.

Detailed Description Text - DETX (2):

The principles of the present invention solve the problem of time lag between the plating and rinse stages by providing a plating cell that performs both plating and full rinse. Performing both plating and full rinse would be undesirable in the prior art plating cell at least because the full rinse would cause rapid dilution of the electroplating solution. The plating cell may also have the ability to perform pre-wetting.

Detailed Description Text - DETX (8):

Electroplating may be performed in circulation mode as follows. In response to an instruction on instruction terminal 199, actuator 170 positions wafer holder 190 so that wafer W is held in solution S, for example, at position 1. A current source 192, disposed within the inner plating bath container 110, emits current through solution S and into wafer W. This causes metal to form on the surface of wafer W as the metal salts within the solution S reduce.

Detailed Description Text - DETX (13):

Once the wafer W has been thoroughly rinsed, the wafer W can be spun to dry at a spin rate of, for example, from 400 to 800 RPM. Therefore, within a very short period after the completion of electroplating, the wafer W is thoroughly rinsed and dried. Therefore, the wafer W is not exposed to corrosive elements as long as the wafer W might be in the prior art.

Detailed Description Text - DETX (15):

Cell 100 may also be used for pre-wetting by spraying a wetting solution (e.g., ultra pure water) onto the wafer W before electroplating while the wafer is positioned over inner plating bath container 110.

United States Patent [19]

Reid et al.

[11] **Patent Number: 6,099,702**

[45] **Date of Patent: Aug. 8, 2000**

[54] **ELECTROPLATING CHAMBER WITH ROTATABLE WAFER HOLDER AND PRE-WETTING AND RINSING CAPABILITY**

[75] Inventors: **Jonathan D. Reid**, Sherwood; **Steven W. Taatjes**, West Linn; **Robert J. Contolini**, Lake Oswego; **Evan E. Patton**, Portland, all of Oreg.

[73] Assignee: **Novellus Systems, Inc.**, San Jose, Calif.

[21] Appl. No.: **09/096,015**

[22] Filed: **Jun. 10, 1998**

[51] **Int. Cl.**[7] **C25D 17/06**; C25D 21/08

[52] **U.S. Cl.** ..... 204/212; 118/52; 118/400; 118/500; 204/224 R; 204/225; 204/237; 204/275

[58] **Field of Search** ..... 205/122; 204/212, 204/224 R, 225, 237, 275; 118/409, 416, 52, 400, 500, 501

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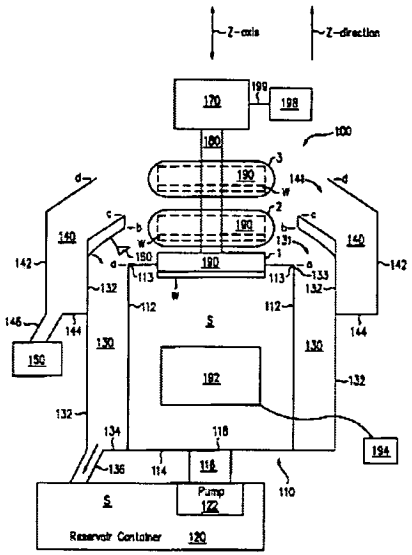
[57] **ABSTRACT**

A plating cell has an inner plating bath container for performing electroplating on a work piece (e.g., a wafer) submerged in a solution contained by the inner plating bath container. A reclaim inlet funnels any solution overflowing the inner plating bath container back into a reservoir container to be circulated back into the inner plating bath container. A waste channel is also provided having an inlet at a different height than the inlet of the reclaim channel. After electroplating, the wafer is lifted to a position and spun. While spinning, the wafer is thoroughly rinse with, for example, ultra pure water. The spin rate and height of the wafer determine whether the water and solution are reclaimed through the reclaim channel or disposed through the waste channel.

10 Claims, 1 Drawing Sheet



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1	US 6187152 B1	21							☑				USPAT
2	US 6183611 B1	21							☑				USPAT
3	US 6165956 A	8							☑				USPAT
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5	US 5965679 A	25						☑					USPAT
6	US 5907791 A	11						☑					USPAT
7	US 5865657 A	22						☑					USPAT

US-PAT-NO: 6165956

DOCUMENT-IDENTIFIER: US 6165956 A

TITLE: Methods and apparatus for cleaning semiconductor substrates after polishing of copper film

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Application Filing Date - AD (1):
19971021

Brief Summary Text - BSTX (6):
One process for Cu metallization uses a dual damascene approach. As illustrated in FIG. 1a, a dielectric layer 110 is deposited above a substrate 100. Dielectric layer 110 may be made up of materials such as silicon dioxide. Vias and/or trenches 120 are then formed in the dielectric layer 110, as illustrated in FIG. 1b. Vias/trenches 120 may be formed, for example, using dry etching techniques. Next, a thin layer of barrier material (barrier layer) 130, for example, tantalum (Ta), titanium (Ti), or titanium nitride (TiN) is deposited as illustrated in FIG. 1c. After barrier layer 130 is deposited the vias/trenches 120 are filled with copper (Cu) layer 140, as illustrated in FIG. 1d. Copper layer 140 may be deposited using well known deposition techniques such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or electroplating . In order to isolate the copper interconnects, as illustrated in FIG. 1e, the excess copper layer 140 and barrier layer 130 must be removed.

Detailed Description Text - DETX (11):
After the second scrub the substrate is then automatically removed from the inside brush station 230 and placed into the rinse, spin and dry station 240. Rinse, spin, and dry station 240 rinses, spins, and dries the substrate. At this point the wafer has been cleaned.

United States Patent [19]

Zhang et al.

[11] **Patent Number: 6,165,956**

[45] **Date of Patent: *Dec. 26, 2000**

[54] **METHODS AND APPARATUS FOR CLEANING SEMICONDUCTOR SUBSTRATES AFTER POLISHING OF COPPER FILM**

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[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

[21] Appl. No.: **08/955,393**

[22] Filed: **Oct. 21, 1997**

[51] **Int. Cl.**[7] C11D 9/04; C11D 17/08; C11D 15/00

[52] **U.S. Cl.** 510/175; 510/176; 510/435; 510/488; 134/2; 134/3

[58] **Field of Search** 510/434, 254, 510/175, 176, 257, 488, 435; 134/3, 41, 2, 28; 528/27

[56] **References Cited**

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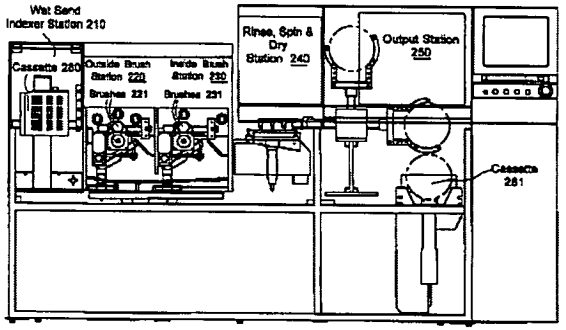
Primary Examiner—Yogendra Gupta
Assistant Examiner—Gregory E. Webb
Attorney, Agent, or Firm—Martine Penilla & Kim, LLP

[57] **ABSTRACT**

A cleaning solution, method, and apparatus for cleaning semiconductor substrates after chemical mechanical polishing of copper films is described. The present invention includes a cleaning solution which combines deionized water, an organic compound, and a fluoride compound in an acidic pH environment for cleaning the surface of a semiconductor substrate after polishing a copper layer. Such methods of cleaning semiconductor substrates after copper CMP alleviate the problems associated with brush loading and surface and subsurface contamination.

1 Claim, 4 Drawing Sheets



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prior to the effective date of the reference(s) or the activity. Such evidence is sufficient because applicant's possession of what is shown carries with it possession of variations and adaptations which would have been obvious, at the same time, to one of ordinary skill in the art. However, the affidavit or declaration showing must still establish possession of the invention (i.e., the basic inventive concept) and not just of what one reference (in a combination of applied references) happens to show, if that reference does not itself teach the basic inventive concept. *In re Spiller*, 500 F.2d 1170, 182 USPQ 614 (CCPA 1974) (Claimed invention was use of electrostatic forces to adhere dry starch particles to a wet paper web on the Fourdrinier wire of a paper-making machine. 37 CFR 1.131 affidavit established use of electrostatic forces to adhere starch particles to wet blotting paper moved over a fluidized bed of starch particles prior to the applied reference date. Affidavit was sufficient in view of prior art reference showing that deposition of dry coatings directly on wet webs on the Fourdrinier wire of a paper-making machine was well known in the art prior to the date of the applied reference. The affidavit established possession of the basic invention, i.e., use of electrostatic forces to adhere starch to wet paper.).

SWEARING BEHIND ONE OF A PLURALITY OF COMBINED REFERENCES

Applicant may overcome a 35 U.S.C. 103 rejection based on a combination of references by showing completion of the invention by applicant prior to the effective date of any of the references; applicant need not antedate the reference with the earliest filing date. However, as discussed above, applicant's 37 CFR 1.131 affidavit must show possession of either the whole invention as claimed or something falling within the claim(s) prior to the effective date of the reference being antedated; it is not enough merely to show possession of what the reference happens to show if the reference does not teach the basic inventive concept.

Where a claim has been rejected under 35 U.S.C. 103 based on Reference A in view of Reference B, with the effective date of secondary Reference B being earlier than that of Reference A, the applicant can rely on the teachings of Reference B to show that the differences between what is shown in his or her 37 CFR 1.131 affidavit or declaration and the claimed invention would have been obvious to one of ordinary skill in the art prior to the date of Reference A. However, the 37 CFR 1.131 affidavit or declaration must still establish possession of the claimed invention, not just what Reference A shows, if Reference A does not teach the basic inventive concept.

GENERAL RULE AS TO GENERIC CLAIMS

A reference or activity applied against generic claims may (in most cases) be antedated as to such claims by an affidavit or declaration under 37 CFR 1.131 showing completion of the invention of only a single species, within the genus, prior to the effective date of the reference or activity (assuming, of course, that the reference or activity is not a statutory bar or a patent, or an application publication, claiming the same invention). See *Ex parte Biesecker*, 144 USPQ 129 (Bd. App. 1964). See, also, *In re Fong*, 288 F.2d 932, 129 USPQ 264 (CCPA 1961); *In re Defano*, 392 F.2d 280, 157 USPQ 192 (CCPA 1968) (distinguishing chemical species of genus compounds from embodiments of a single invention). See, however, MPEP § 715.03 for practice relative to cases in unpredictable arts.

715.03 Genus-Species, Practice Relative to Cases Where Predictability Is in Question

→ Where generic claims have been rejected on a reference or activity which discloses a species not antedated by the affidavit or declaration, the rejection will not ordinarily be withdrawn, subject to the rules set forth below, unless the applicant is able to establish

that he or she was in possession of the generic invention prior to the effective date of the reference or activity. In other words, the affidavit or declaration under 37 CFR 1.131 must show as much as the minimum disclosure required by a patent specification to furnish support for a generic claim.

REFERENCE OR ACTIVITY DISCLOSES SPECIES

A. Species Claim

Where the claim under rejection recites a species and the reference or activity discloses the claimed species, the rejection can be overcome under 37 CFR 1.131 directly by showing prior completion of the claimed species or indirectly by a showing of prior completion of a different species coupled with a showing that the claimed species would have been an obvious modification of the species completed by applicant. See *In re Spiller*, 500 F.2d 1170, 182 USPQ 614 (CCPA 1974).

B. Genus Claim

The principle is well established that the disclosure of a species in a cited reference is sufficient to prevent a later applicant from obtaining a "generic claim." *In re Gosteli*, 872 F.2d 1008, 10 USPQ2d 1614 (Fed. Cir. 1989); *In re Slayter*, 276 F.2d 408, 125 USPQ 345 (CCPA 1960).

Where the only pertinent disclosure in the reference or activity is a single species of the claimed genus, the applicant can overcome the rejection directly under 37 CFR 1.131 by showing prior possession of the species disclosed in the reference or activity. On the other hand, a reference or activity which discloses several species of a claimed genus can be overcome directly under 37 CFR 1.131 only by a showing that the applicant completed, prior to the date of the reference or activity, all of the species shown in the reference. *In re Stempel*, 241 F.2d 755, 113 USPQ 77 (CCPA 1957).

Proof of prior completion of a species different from the species of the reference or activity will be sufficient to overcome a reference indirectly under 37 CFR 1.131 if the species shown in the reference or activity would have been obvious in view of the species shown to have been made by the applicant. *In re Clarke*, 356 F.2d 987, 148 USPQ 665 (CCPA 1966); *In re Plumb*, 470 F.2d 1403, 176 USPQ 323 (CCPA 1973); *In re Hostettler*, 356 F.2d 562, 148 USPQ 514 (CCPA 1966). Alternatively, if the applicant cannot show possession of the species of the reference or activity in this manner, the applicant may be able to antedate the reference or activity indirectly by, for example, showing prior completion of one or more species which put him or her in possession of the claimed genus prior to the reference's or activity's date. The test is whether the species completed by applicant prior to the reference date or the activity's date provided an adequate basis for inferring that the invention has generic applicability. *In re Plumb*, 470 F.2d 1403, 176 USPQ 323 (CCPA 1973); *In re Rainer*, 390 F.2d 771, 156 USPQ 334 (CCPA 1968); *In re Clarke*, 356 F.2d 987, 148 USPQ 665 (CCPA 1966); *In re Shokal*, 242 F.2d 771, 113 USPQ 283 (CCPA 1957).

It is not necessary for the affidavit evidence to show that the applicant viewed his or her invention as encompassing more than the species actually made. The test is whether the facts set out in the affidavit are such as would persuade one skilled in the art that the applicant possessed so much of the invention as is shown in the reference or activity. *In re Schaub*, 537 F.2d 509, 190 USPQ 324 (CCPA 1976).

C. Species Versus Embodiments

References or activities which disclose one or more embodiments of a single claimed invention, as opposed to species of a claimed genus, can be overcome by filing a 37 CFR 1.131 affidavit showing prior completion of a single embodiment of the invention, whether it is the same or a different embodiment from that disclosed in the reference or

activity. See *In re Fong*, 288 F.2d 932, 129 USPQ 264 (CCPA 1961) (Where applicant discloses and claims a washing solution comprising a detergent and polyvinylpyrrolidone (PVP), with no criticality alleged as to the particular detergent used, the PVP being used as a soil-suspending agent to prevent the redeposition of the soil removed, the invention was viewed as the use of PVP as a soil-suspending agent in washing with a detergent. The disclosure in the reference of the use of PVP with two detergents, both of which differed from that shown in applicant's 37 CFR 1.131 affidavit, was considered a disclosure of different embodiments of a single invention, rather than species of a claimed genus); *In re Defano*, 392 F.2d 280, 157 USPQ 192 (CCPA 1968).

REFERENCE OR ACTIVITY DISCLOSES CLAIMED GENUS

In general, where the reference or activity discloses the claimed genus, a showing of completion of a single species within the genus is sufficient to antedate the reference or activity under 37 CFR 1.131. *Ex parte Biesecker*, 144 USPQ 129 (Bd. App. 1964). In cases where predictability is in question, on the other hand, a showing of prior completion of one or a few species within the disclosed genus is generally not sufficient to overcome the reference or activity. *In re Shokal*, 242 F.2d 771, 113 USPQ 283 (CCPA 1957). The test is whether the species completed by applicant prior to the reference date or the date of the activity provided an adequate basis for inferring that the invention has generic applicability. *In re Mantell,* 454 F.2d 1398, 172 USPQ 530 (CCPA 1973); *In re Rainer*, 390 F.2d 771, 156 USPQ 334 (CCPA 1968); *In re DeFano*, 392 F.2d 280, 157 USPQ 192 (CCPA 1968); *In re Clarke*, 356 F.2d 987, 148 USPQ 665 (CCPA 1965). In the case of a small genus such as the halogens, which consists of four species, a reduction to practice of three, or perhaps even two, species might show possession of the generic invention, while in the case of a genus comprising hundreds of species, reduction to practice of a considerably larger number of species would be necessary. *In re Shokal, supra.*

It is not necessary for the affidavit evidence to show that the applicant viewed his or her invention as encompassing more than the species he or she actually made. The test is whether the facts set out in the affidavit are such as would persuade one skilled in the art that the applicant possessed so much of the invention as is shown in the reference. *In re Schaub*, 537 F. 509, 190 USPQ 324 (CCPA 1976).

715.04 Who May Make Affidavit or Declaration; Formal Requirements of Affidavits and Declarations

WHO MAY MAKE AFFIDAVIT OR DECLARATION

The following parties may make an affidavit or declaration under 37 CFR 1.131:

(A) All the inventors of the subject matter claimed.

(B) An affidavit or declaration by less than all named inventors of an application is accepted where it is shown that less than all named inventors of an application invented the subject matter of the claim or claims under rejection. For example, one of two joint inventors is accepted where it is shown that one of the joint inventors is the sole inventor of the claim or claims under rejection.

(C) A party qualified under 37 CFR 1.42, 1.43, or 1.47 in situation where some or all of the inventors are not available or not capable of joining in the filing of the application.

(D) The assignee or other party in interest when it is not possible to produce the affidavit or declaration of the inventor. *Ex parte Foster*, 1903 C.D. 213, 105 O.G. 261 (Comm'r Pat. 1903).

Affidavits or declarations to overcome a rejection of a claim or claims must be made